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01 FC:1501 02 FC:1504	1370.00 OP 300.00 OP				Sim	11-17-04	(Date)
APPLICATION NO.	FILING DATE	FIRST NAMED INVE		INVEN	TOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,308	03/03/2004	Paolo Cappellett				96-AG-114 (19321-DIV2	4643
TITLE OF INVENTION: ! LAYER GATE DIELECTR APPLN. TYPE		LOATING GATE			MEMORY CELL WI	TH LOW ERASING VOI	TAGE HAVING DOUBLE
nonprovisional	NO NO				\$300	\$300	12/27/2004
nonprovisional	nonprovisional		\$PX 1370		\$300	\$1670	12/2//2004
EXAMINER		ART UNIT		CL	ASS-SUBCLASS		
NGUYEN, CU	ONG QUANG	2811	•		438-257000		
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SGS-Thomso	on Microelectronics	S.r.l.	Α	grate	Brianza, Italy	,	
	assignee category or categor	ries (will not be pri	nted on the pa	tent) :	Individual 🚨 C	orporation or other private g	group entity Government
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Authorized Signature	JEL Ch	any			Date	11-17-04 1No. 32,180	
Typed or printed name _	RICHARD K. W	ARTHER			Registration	No. <u>32,180</u>	
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